Please replace the last paragraph on page 7, beginning at line 22, with the following clean replacement paragraph:

Fig. 1 depicts but one preferred implementation of the invention in a method of forming non-volatile random access memory circuitry. A plurality of memory cell access transistor gates 14, 16, 18 and 20 are formed over semiconductor substrate 12. By way of example only, such comprise a gate dielectric layer 22, an overlying conductively doped polysilicon layer 24, an overlying conductive metal silicide layer 26, an insulative cap 28, and opposing anisotropically etched insulative sidewall spacers 29. In the depicted preferred embodiment, gate constructions 14-20 are in the form of memory cell wordlines. Substrate isolation, for example LOCOS field isolation oxide or trench isolation, is not shown for clarity, and as not constituting particular materiality to the invention. Discussion proceeds with processing particularly material to memory cell wordlines 16 and 18 which are proximate one another.

Please replace the first complete paragraph on page 13, beginning at line 3, with the following clean replacement paragraph:

Such provides but a few examples of forming integrated circuitry, such as memory circuitry, in accordance with but some aspects of the invention, with memory cells 54 and 56 constituting but exemplary memory cell storage devices comprising voltage or current controlled resistance setable semiconductive material. Yet in one aspect, the invention comprises a method of forming any memory circuitry which sequentially comprises the formation of some plurality of metal interconnect lines over a semiconductive substrate followed by the formation of a plurality of memory cell storage devices comprising voltage or current controlled resistance setable semiconductive material. Further considered, the invention comprises any method of forming integrated circuitry (whether existing or yet-to-be-developed) which sequentially comprises forming at least one metal interconnect line over a semiconductive substrate followed by the formation of any device comprising two metal comprising electrodes separated by a voltage or current controlled resistance setable semiconductive material.

Please replace the last paragraph on page 13, beginning at line 17, with the following clean replacement paragraph:

These and other aspects of the invention are also considered and contemplated by way of example only with respect to but one exemplary alternate embodiment depicted in Figs. 3-8. Fig. 3 depicts a wafer fragment 60 comprising a bulk semiconductive substrate 62 having an exemplary shallow trench field isolation region 64 formed therein. Various exemplary conductive device components 66, 68, 70, 72, 74 and 76 are shown as being formed over substrate 62. Such might constitute completed devices or devices in fabrication in the form of conductive lines, such as interconnect lines or field effect transistor lines, or any other conductive device or component thereof. By way of illustration and example only, such device components are depicted as having conductive polysilicon portions 77, overlying metal portions 79, and insulative silicon nitride caps 78. A dielectric layer 80 has been deposited, and planarized back. An exemplary silicon nitride layer 82 is formed thereover. Exemplary contact openings have been formed through layers 82 and 78 with respect to conductive device components 66, 68, 70, 74 and 76.